REMARKS

1. Double Patenting Rejection

The Applicant hereby files the enclosed Terminal Disclaimer with 3.73(b) Statement.

2. § 112 Second Paragraph Rejection

Claim 1 has been amended to avoid the § 112 basis for rejection by inserting -- first – before the fist occurrence of "binary sequences;" by inserting – first plurality of – before the second occurrence of "binary sequencing;" and by inserting – controller – before "shift register."

In relation to the Examiner's § 112 rejection to the phrase "a plurality of nonlinear function generators having said binary sequences as their input," the phrase is clear when read in conjunction with the description as is intended of claims. Paragraphs [0033], [0034] (pages 8 and 9 of the specification) and Figures 2 and 4 make it clear that the output N of the Linear Feedback Shift Registers 18 is an n-bit signal and the input of each Boolean function 19 is n-bits. Thus, each bit of the first plurality of binary sequences feeds into each of the plurality of nonlinear function generators.

3. § 112 First Paragraph Rejection (Claims 1, 2, and 10)

In paragraph 5, the Examiner contends that Claims 1 and 2 are not enabled by the description because it is not clearly pointed out how to form K1 and K2. Once the requirements of the arrangement are known, the answer is very clear. A multiplexer is a very common component in IC form that switches a multi-bit input to a single output. All common multiplexer IC's have three inputs, namely, a multi-bit data input, a single data output, and a control input. One input bit is selected at a time, and the selected input is transmitted to the single output. The selected input is based on a binary number at the control input. This most rudimentary principle of multiplexer operation is well known in the art, even to students. A shift register is similarly a very rudimentary device. The one skilled in the art would have no trouble ascertaining the required arrangement form the drawings an description. Figure 1 shows the overall connection of the multiplexer within the device. Taking, for example, MUX 1, it has at its

input the multi-bit (m-bit input) signal M1 from Function Generator A. See Figure 4. Its single output goes to the first bit of the controller which is implemented as shift register of k memory elements 20. See Figure 5. An output K1 of the shift register is connected to the multiplexer control input. This output K1 is a binary sequence form the shift register as shown in Figure 5. Thus, the controller including a shift register is operable to control the first and second switches (MUXs) and the first switch (MUX 1) Is operative to select one of said second plurality of binary sequencers (M1) to the first big of the (controller) shift register.

In relation to Claim 10, the above discussion about the MUXs and controller (shift register) makes this claim clear also. The output sequence is the output 17 of MUX 2, which is controlled by the shift register output K2. The shift register input is randomized by applying to it one of the second plurality of binary sequences via MUX 1, which in turn is controlled by the shift register (output K1).

Attached is a Declaration from one of the inventors, Dr. Cheng, an expert in this field responding to the Examiner's continued rejection of Claims 1-10, over the three citations to Beker, Roth, and Puhl. All of the independent claims (1, 2, and 7) require through their language a structural arrangement of a **linear feedback shift register** connected to **nonlinear function generators** connected to **first and second switches (e.g. MUXs or multiplexers)**. The Applicant's position is that the combination of the three citations does not meet the strict requirement of teaching every claimed element. In particular, if one were to combine Beker, Roth, and/or Puhl, one would not get **at least first and second switches** so that **the first switch operative to select one of said second plurality of binary sequences to the first bit of the shift register, and the second switch operative to select one of said second plurality of binary sequences to an output**. This is essential to the invention as will become apparent from Dr. Cheng's comments. Beker shows **linear feedback shift registers** connected to **a (one) switch** (i.e., a multiplexer). Roth shows **linear feedback shift registers** connected to a **nonlinear function generator**. The nonlinear function is created by feeding the

generator output back to its input with a delay function. In his Declaration, Dr. Cheng states that if one simply puts the **nonlinear function generator** taught by Roth between the **linear feedback shift register** LSFB T and **multiplexer** of Beker, the resulting device would not work because the correlation between the control data for the multiplexer (LSFR S in Beker) and the multiplexer input data (the **nonlinear function generator output** replacing LSFB T connected to multiplexer inputs B0 – B32) restricts the randomness of the output.

The current invention teaches how to overcome this problem by having the output of the LSFR fed into two function generators connected to two switches, the output of the first function generator and switch providing an input to the controller, and the output of the second function generator and second switch providing the randomized output. That there is at least two (i.e., a plurality of) non-linear function generators and at least two switches is essential to the invention and this is not taught by any combination of the citations.

Additionally, the applicant would further re-present the arguments offered to the Examiner in the reply filed 30 March 2006:

a) The Examiner's position is that Figure 1 of Beker shows a first switch and Figure 3 of Beker shows a second switch (a MUX being equivalent to a switch). However, there is only one switch (MUX) in the system of Beker. The Figures 1, 2 and 3 of Beker are not cumulative, but are variants of the same system which is an arrangement of logic gates used to construct a linear feedback shift register. The logic gates are connected to a single multiplexer (M). Thus, Beker does not disclose first and second switches.

The Examiner's position is that Figure 1 of Beker shows a plurality of linear feedback shift registers and Figures 1 and 3 of Beker also show a controller including a shift register operable to control the first and second switches. The Examiner argues that the controller of figure 1 is on the left and the controller of Figure 3 is at the top. The Examiner is confused. In figure 1 the group of logic gates at the top form a first linear feedback shift register (LFSR T) and the group of logic gates on the left form a second linear feedback shift register (LFSR S).

Figure 1 can therefore not show a plurality of linear feedback shift registers and a controller as this requires at least three elements when only two elements are present in that drawing. Again Figure 3 cannot be additional to figure 1 to disclose the additional element as Figure 3 is clearly described as an alternative in the description. According to the description at the top of column 4 of Beker Figure 3 shows only one linear feedback shift register comprising the two rows of logic gates at the top of Figure 3. Thus Figure 3 only comprises a multiplexer and one other element and so cannot disclose a plurality of linear feedback shift registers and a controller.

Thus, the combination of Beker with both Roth and Puhl cannot disclose every element of Claims 1 and 2 as believed by the Examiner.

b) The Examiner is further of the view that Beker does not teach a plurality of nonlinear functions, but that Roth teaches a plurality of nonlinear function having a binary sequence as their input. The output from the linear feedback shift registers is summed in the sigma block to form a signal output. However, the Applicant can see no motivation in either Roth or Beker for combining the teachings, nor any expectation of success in doing so. Insufficient information is given in Beker and Roth to combine the teachings successfully in the way required by the claim. At the bottom of column 1 lines 63 to 68, Beker requires that during normal running the last stage in each shift register is applied to the input of the first stage in a re-circulating loop. The multiplexer has connections to various intermediate states of the shift register. Thus, it would not be clear to the skilled-addressee at which stage the nonlinear function should be applied in order to generate the second plurality of binary sequences, nor where the second plurality of binary sequences is selected by a multiplexer. Substantial alteration of the system of Beker would be required to accommodate the teachings of Roth.

c) Claim 7 is rejected for being unpatentable over Roth in view of Beker. The Examiner's position is that Roth teaches all of the elements of the claim except selecting an output sequence from one of the plurality of binary sequences, but that Beker teaches this in Figure 1. Claim 7 recites "randomly selecting an output sequence from one of the second plurality

of binary sequences." Beker does not disclose randomly selecting an output sequence. Beker discloses applying the output sequence from each shift register to the input of the first stage in a re-circulating loop [column 1 lines 63 to 68]. Thus, the combination of Beker and Roth does not disclose every element of Claim 7.

All the dependent claims are novel and patentable over Beker, Roth and Puhl for the same reasons, and the Applicant asks the Examiner to reconsider the claims and issue a Notice of Allowance.

Respectfully submitted,
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